Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1(currently amended): A method of forming a silicon thin film comprising the steps of:

providing a substrate[[,]];

forming an amorphous silicon (a-Si) pattern ~~being comprised~~ on the substrate, [[and]]wherein the amorphous silicon pattern comprising:

a first region having a first height;

a second region having the first height;

at least one first pointed region being adjacent to the second region, each first pointed region having a second height;

a third region, the third region being located between the first region and the second region, each first pointed region being located on the third region, the third region having a third height; and

at least one fourth region, each fourth region being located on the third region between the first region and each first pointed region, each fourth region having a fourth height smaller than the second height and greater than the third height; and

performing the laser crystallization process to allow an amorphous silicon seed in each first pointed region adjacent to each fourth region to grow and to crystallize as a first single crystal silicon grain in each fourth region.

Claim 2(original): The method of claim 1 wherein the substrate comprises a glass substrate, a quartz substrate, or a plastic substrate.

Claim 3(original): The method of claim 1 wherein the first height is substantially equal to the sum of the second height and the third height.

Claim 4(original): The method of claim 1 wherein a second pointed region is comprised between the first region and each fourth region, and each second pointed region has a fifth height greater than the fourth height.

Claim 5(original): The method of claim 4 wherein the first height is substantially equal to the sum of the fifth height and the third height, and the third height is smaller than the fourth height.

Claim 6(original): The method of claim 4 wherein an amorphous silicon seed in each second pointed region adjacent to each fourth region grows to crystallize as a second single crystal silicon grain in each fourth region when the laser crystallization process is performed.

Claim 7(original): The method of claim 1 wherein the laser crystallization process is to irradiate the amorphous silicon pattern with a laser pulse to completely melt the amorphous silicon thin film in each fourth region and to partially melt the amorphous silicon thin film in each first pointed region so that the residual solid silicon in each first pointed region adjacent to each fourth region becomes a site of nucleation to perform super lateral growth (SLG).

Claim 8(original): The method of claim 7 wherein the temperature of the third region not covered by each fourth region and each first pointed region is higher than the temperature of each fourth region so that each site of nucleation grows from each fourth region toward the third region not covered by each fourth region and each first pointed

region after the amorphous silicon pattern is irradiated by the laser pulse.

Claim 9(original): The method of claim 8 wherein the laser crystallization process is to irradiate the amorphous silicon pattern with the laser pulse to completely melt the amorphous silicon thin film in the third region not covered by each fourth region and each first pointed region and to partially melt the amorphous silicon thin film in the first region and the second region so that a plurality of amorphous silicon seeds in the first region and the second region grow to crystallize as polysilicon grains in the third region not covered by each fourth region and each first pointed region.

Claim 10(original): The method of claim 1 wherein the amorphous silicon thin film in the third region covered by each fourth region and each first pointed region is partially melted after the laser crystallization process is performed.

Claim 11(original): The method of claim 1 wherein the laser comprises an excimer laser, a gas pulse laser, a solid pulse laser, or a continuous wave laser.

Claim 12(currently amended): The method of claim 1 further comprising the following steps after performing the laser crystallization process:

forming at least one gate insulating layer on each fourth region; and

forming at least one patterned gate electrode on the gate insulating layer on each fourth region[[;]].

Claim 13(original): The method of claim 12 wherein the first region and the second region are a source/drain region of a thin film transistor, and the fourth region is a channel region of the thin film transistor.

Claim 14(original): The method of claim 13 further comprising the following steps

after forming each gate electrode:

performing an ion implantation process to form source/drain electrodes of the thin film transistor in the first region and the second region by utilizing each of the gate electrodes as a mask; and

performing an activation process to activate the dopants in the source/drain electrodes of the thin film transistor.

Claim 15(original): The method of claim 13 wherein the thin film transistor is a low temperature polysilicon thin film transistor (LTPS TFT).

Claim 16(original): The method of claim 12 further comprising the following steps when forming each gate insulating layer:

performing at least one plasma enhanced chemical vapor deposition (PECVD) process to form at least one dielectric layer on the substrate.

Claim 17(original): The method of claim 16 wherein the material composition of each dielectric layer comprises silane-based silicon oxide, tetra-ethyl-ortho-silicate based silicon oxide, silicon nitride, or silicon oxynitride.

Claim 18(original): The method of claim 12 wherein the material composition of each gate electrode comprises tungsten (W), chrome (Cr), or other conductive metal.

Claim 19(new): A method of forming a silicon thin film comprising the steps of:

providing a substrate;

forming an amorphous silicon (a-Si) pattern on the substrate wherein the amorphous silicon pattern comprising:

a first region having a first height;

a second region having the first height;

at least one first pointed region being adjacent to the second region, each first pointed region having a second height;

a third region, the third region being located between the first region and the second region, each first pointed region being located on the third region, the third region having a third height;

at least one fourth region, each fourth region being located on the third region between the first region and each first pointed region, each fourth region having a fourth height smaller than the second height and greater than the third height;

performing the laser crystallization process to allow an amorphous silicon seed in each first pointed region adjacent to each fourth region to grow and to crystallize as a first single crystal silicon grain in each fourth region;

forming at least one gate insulating layer on each fourth region; and

forming at least one patterned gate electrode on the gate insulating layer on each fourth region.

Claim 20(new): The method of claim 19 wherein the first region and the second region are a source/drain region of a thin film transistor, and the fourth region is a channel region of the thin film transistor.

Claim 21(new): The method of claim 20 further comprising the following steps after forming each gate electrode:

performing an ion implantation process to form source/drain electrodes of the thin film transistor in the first region and the second region by utilizing each of the gate electrodes as a mask; and

performing an activation process to activate the dopants in the source/drain electrodes of the thin film transistor.

Claim 22(new): The method of claim 20 wherein the thin film transistor is a low temperature polysilicon thin film transistor (LTPS TFT).

Claim 23(new): The method of claim 19 further comprising the following steps when forming each gate insulating layer:

performing at least one plasma enhanced chemical vapor deposition (PECVD) process to form at least one dielectric layer on the substrate.

Claim 24(new): The method of claim 23 wherein the material composition of each dielectric layer comprises silane-based silicon oxide, tetra-ethyl-ortho-silicate based silicon oxide, silicon nitride, or silicon oxynitride.

Claim 25(new): The method of claim 19 wherein the material composition of each gate electrode comprises tungsten (W), chrome (Cr), or other conductive metal.